Impact of On-Chip Interconnect on the Performance of 3-D Integrated Circuits With Through-Silicon Vias: Part II

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***Abstract*— 3-D integration using through-silicon vias (TSVs) can decrease interconnect length and improve chip performance. In this paper, electrical links consisting of TSVs and horizontal wires are designed, fabricated, and measured to analyze TSV capacitance and link delay. Compact models for the capacitance of a TSV surrounded by variable number of ground TSVs are developed and compared with measurements. The impact of TSV placement and scaling on link performance is further analyzed. The results demonstrate that placing TSVs closer to their drivers can effectively improve the performance of 3-D integrated circuit (3-D IC) links. Moreover, link delay is significantly improved by scaling TSV geometry to the point that 3-D IC links become on-chip wire limited.**

***Index Terms*— 3-D integrated circuit (3-D IC), 3-D integration, fabrication, interconnect, measurement, modeling, through-silicon via (TSV).**

I. Introduction

THE demand for dense, low-energy, and high-bandwidth interconnects continues to grow in both high-performance and mobile applications [1], [2]. Through-silicon via (TSV)-based 3-D integrated circuits (3-D ICs) have become a promising solution for high-bandwidth and high-density heterogeneous systems [3]–[5]. One of the advantages of TSV-based 3-D ICs is the ability to realize high-density short vertical interconnects [6], [7], which lead to high bandwidth density and low energy-per-bit signaling.

Even though it is appealing, the integration of TSVs introduces new challenges. Prior research has focused on the fabrication technology [8], [9], mechanical [10], thermal [11], and electrical attributes of 3-D ICs. The electrical properties of TSVs are of particular interest. Experimental analysis of 3-D IC links, including wires and TSVs, has been reported [12], [13], but the interconnects were designed for interposer applications and therefore, contained much larger dimensions than those suited for on-chip applications. Other experimental efforts addressed the I/O circuitry rather than the interconnects [14]. Thus, there is a need to further experimentally explore how TSVs and on-chip wires impact the overall performance of 3-D IC links.

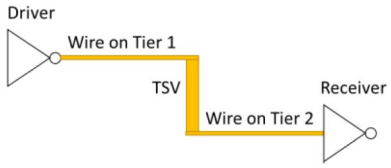

Fig. 1. Two tier simple 3-D IC link.

In this paper, TSV arrays and 3-D IC links with TSVs and horizontal wires (representing on-chip wires) are fabricated, measured, and analyzed. The models presented in Part I of this paper are compared with measurements. In Section II, the delay model for 3-D IC electrical links developed in Part I is briefly introduced along with an analytical model for TSV capacitance. Section III summarizes the experimental design and the fabrication process. Section IV is divided into two parts: the first part compares the TSV capacitance model to the measurements and the second part reports 3-D IC link analysis including eye-diagrams and link delay. The link delay model is verified for various wire lengths. Moreover, the impact of TSV diameter scaling is analyzed using the experimentally verified models. Finally, conclusions are presented in Section V.

II. Analytical Models for 3-D IC Links and TSV Capacitance

A simple link in a 3-D IC is shown in Fig. 1. The 50%–50% delay of the link can be calculated using the Elmore delay model [15]

$$\begin{aligned}\tau_{50\%-50\%} &= 0.69\left(R_{dr}+r_{tx}L_{tx}\right)C_{\text{tsv}}\\ &\quad+0.69R_{dr}\left(c_{tx}L_{tx}+c_{rx}L_{rx}+C_{rx}+C_{dr}\right)\\ &\quad+0.69r_{tx}c_{rx}L_{tx}L_{rx}\\ &\quad+0.38\left(r_{tx}c_{tx}L_{tx}^2+r_{rx}c_{rx}L_{rx}^2\right)\end{aligned} \tag{1}$$

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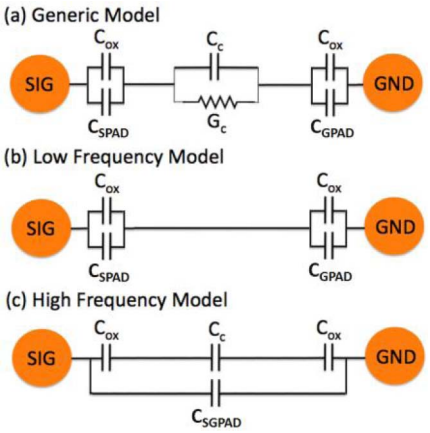

Fig. 2. TSV capacitance circuit models showing the capacitance between signal and ground TSVs at (a) any frequency, (b) low frequency, and (c) high frequency.

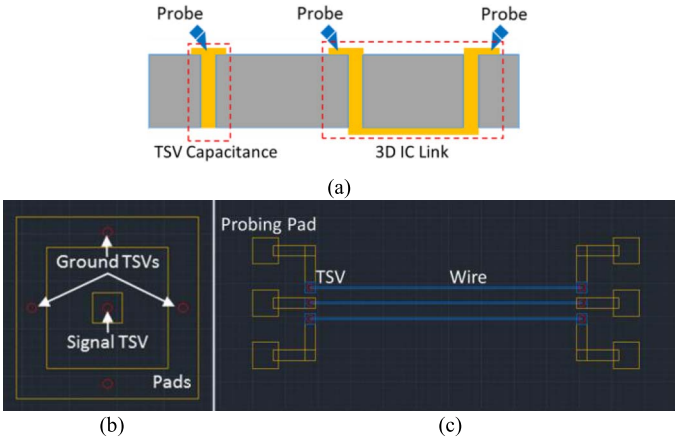

Fig. 3. Experimental design for TSV capacitance and TSV-wire-TSV 3-D IC link measurements. (a) Design overview of TSV capacitance and 3-D IC link measurements. (b) TSV capacitance design: one signal TSV with different number of ground TSVs for TSV capacitance extraction. (c) 3-D IC link design: the link with probing pads, TSVs, and wires on the back side.

where R_{dr} and C_{dr} are the driver resistance and capacitance, respectively, r_{tx}, c_{tx}, and L_{tx} are the resistance per unit length, the capacitance per unit length, and the length of the on-chip wire on the driver side (Tier 1 in Fig. 1), respectively, and r_{rx}, c_{rx} and L_{rx} are the same for the on-chip wire on the receiver side (Tier 2 in Fig. 1). C_{tsv} is the capacitance of the TSV, and C_{rx} is the load capacitance of the receiver.

The first term in (1), i.e., the delay due to the driver side resistance combined with the TSV capacitance, dominates the total delay. Therefore, it is very important to understand and accurately model the TSV capacitance.

A circuit model for two TSVs in a TSV array is shown in Fig. 2(a). This model is simplified for low- and high-frequency cases. Due to the metal–insulator–semiconductor structure, TSVs may operate at either slow-wave mode or quasi-TEM mode depending on the frequency, TSV dimensions, and substrate resistivity [16]. When the operating frequency is lower than 0.3 times the characteristic frequency of the slow-wave mode ($0.3 f_{\text{sw}}$) [17], which is typically in the kilohertz and megahertz range, the TSV is in the slow-wave mode. In this mode, TSV capacitance is mainly determined by its oxide capacitance, which we define as the low-frequency capacitance. As frequency increases, there is a transition from the slow-wave mode to the quasi-TEM mode, allowing complete penetration of the E-field and H-field through the silicon substrate [17], [18]. In this mode, the TSV capacitance is saturated by the silicon substrate capacitance C_c in Fig. 2(c). In our simulation, the quasi-TEM mode is observed at frequencies higher than ∼10 GHz (depending on TSV dimensions). In this mode, the overall TSV capacitance is constant and equal to C_c. In this paper, we assume that the substrate is floating and is not biased during the measurement.

The admittance of the substrate between two TSVs can be calculated as [19]

$$Y = G_C + j2\pi f C_c \tag{2}$$

where G_C is the substrate conductance and f is the frequency of operation. At low frequencies, G_C dominates the admittance. Therefore, the substrate capacitance is shorted out, reducing the model to the one shown in Fig. 2(b). As a result, the TSV capacitance to the substrate is approximately the TSV liner capacitance. Depending on the number of ground TSVs surrounding the signal TSV, including the pad capacitances, the effective low-frequency capacitance is given by

$$C_{\text{LF}} = \frac{1}{\left(\frac{1}{N_{\text{GND}} C_{\text{OX}} + C_{\text{GPAD}}}\right) + \left(\frac{1}{C_{\text{OX}} + C_{\text{SPAD}}}\right)} \tag{3}$$

where C_{OX} is the TSV liner capacitance, C_{GPAD} is the capacitance from the ground pad to the substrate, C_{SPAD} is the capacitance from the signal pad to the substrate, and N_{GND} is the number of ground TSVs surrounding the signal TSV.

At high frequencies, the capacitive admittance is much larger relative to the conductance of the substrate. As a result, the conductance of the substrate is ignored, as shown in Fig. 2(c). The substrate capacitance (C_c) for each of the TSV array configurations is estimated using Synopsys Raphael [20]. The effective high-frequency capacitance as a function of the TSV array configurations is given by

$$C_{\text{HF}} = \frac{1}{\left(1 + \frac{1}{N_{\text{GND}}}\right)\left(\frac{1}{C_{\text{OX}}}\right) + \frac{1}{C_c}} + C_{\text{SGPAD}} \tag{4}$$

where C_{HF} is the high-frequency capacitance, and C_{SGPAD} is the capacitance from the signal to ground pads.

III. Experiment Design and Fabrication

Two design sets for the experimental evaluation of TSVs and on-chip wires are illustrated in Fig. 3. For TSV capacitance extraction, single-port measurements are used, while for TSV-wire-TSV 3-D IC links, two-port measurements are used. The dimensions of all interconnect structures are summarized in Table I.

A. TSV Capacitance Extraction

Six designs are fabricated to extract the capacitance of TSVs, as shown in Fig. 4. Each design contains one signal

TABLE I
DIMENSIONS OF STRUCTURES

Structure	Dimensions
TSV	Diameter = 14 μm, Pitch = 30 μm (3D IC link), 50 μm, 100 μm (TSV capacitance), Height = 300 μm, Liner thickness = 0.4 μm
Wire	Length = 0.5 mm, 1 mm, 2 mm, 4 mm, 8 mm
	Width = 3 μm, Pitch = 30 μm, Thickness = 0.1 μm
Probing pads	Width = 40 μm, Pitch = 100 μm, Thickness = 0.6 μm

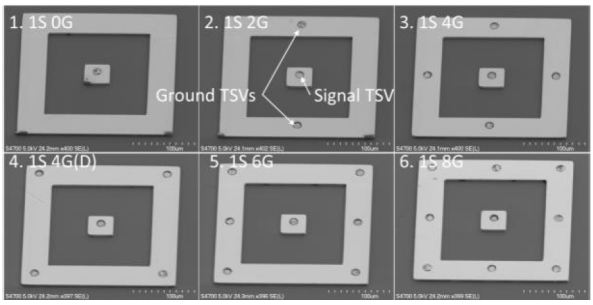

Fig. 4. SEM images of six TSV sets with various number of ground TSVs ranging from 0 to 8 (1S 0G indicates one signal TSV and zero ground TSV).

TSV in the center surrounded by various number of ground TSVs with a shorted probe pad. The first TSV design consists of no ground TSVs to characterize the capacitance of the signal TSV to the ground pad as a reference to the other designs (top-left image of Fig. 4). The number of ground TSVs in the second through sixth designs is 2, 4, 4, 6, and 8, respectively. The third and fourth designs both have four ground TSVs, but their positions are different to compare diagonal TSVs to nearby TSVs. The impact of TSV pitch is also investigated by fabricating all six designs with TSV pitches of 50 and 100 μm.

B. 3-D IC Link

Coplanar waveguide configured ground-signal-ground wires are used to emulate on-chip wires. The dimensions of the structures were selected to emulate the electrical parameters of a 3-D IC link based on the ITRS 2013 report [21]. The wire pitch is selected to be the same as the TSV pitch for design and analysis simplicity. Differing wire and TSV pitches require fan-in/fan-out structures on both ends of the wire, which introduce discontinuities and impact the accuracy of the L-2L de-embedding.

The fabrication process begins with a 300-μm thick double-side polished silicon wafer. Silicon dioxide is deposited on the top side of the wafer using plasma-enhanced chemical vapor deposition and patterned using dry etching. The silicon vias are then etched using the Bosch process with silicon dioxide as the mask. Following the Bosch process, the wafer is immersed in buffered oxide etchant to remove the silicon dioxide. Next, a liner of silicon dioxide is thermally grown. A seed layer of titanium and copper is then deposited on the back side using electron beam evaporation, followed by a bottom-up copper electroplating. The over-electroplated copper is removed by chemical-mechanical polishing to expose the TSVs. Finally, probe pads and wires are patterned on the front and back sides of the wafer, respectively. The fabrication process is summarized in Fig. 5.

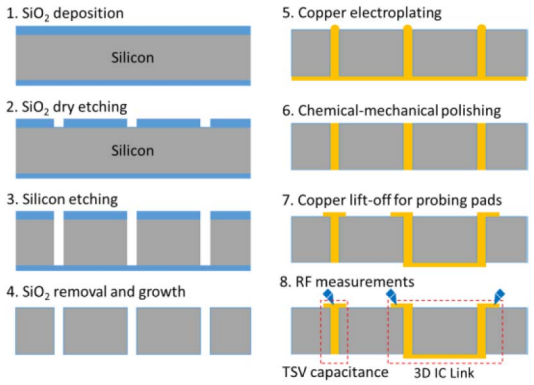

Fig. 5. Overall fabrication process for TSV capacitance extraction and 3-D IC link characterization.

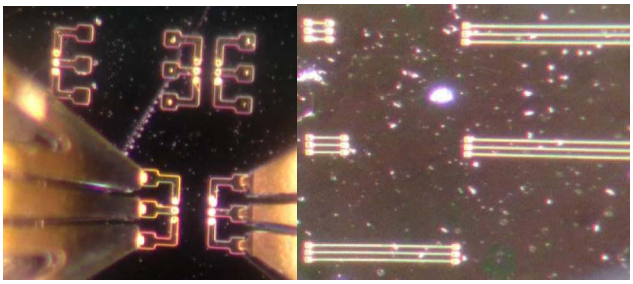

Fig. 6. Images of the tested samples. (a) Front side of the sample on the probing station, where the bright dots on the end of the probing pads are TSVs. (b) Back side of the sample with the fine wires. The surface of the sample is slightly damaged by chemical-mechanical polishing (CMP).

The overall wire thickness is 100 nm, including 30-nm-thick titanium, 50-nm-thick copper, and 20-nm-thick gold. Optical images of the fabricated testbed are shown in Fig. 6.

IV. RESULT ANALYSIS

The fabricated testbed is measured using an Agilent N5245A network analyzer to obtain the S-parameters from 10 MHz to 50 GHz at a 250 MHz step. Single port S_{11} parameters are measured for TSV capacitance extraction. For 3-D IC link measurements, 2-port S-parameters are measured. The probe pads are de-embedded using L-2L de-embedding [22]. Finally, the S-parameters are imported into Keysight Advanced Design System (ADS) [23] to extract the time-domain response of the links.

A. TSV Capacitance

For each of the TSV array configurations described in the previous section, the experimentally obtained values of capacitance are compared with those extracted through HFSS and analytical/extracted models. Error bars are added to the modeled capacitance to reflect TSV diameter variation of ± 1 μm due to fabrication process variation.

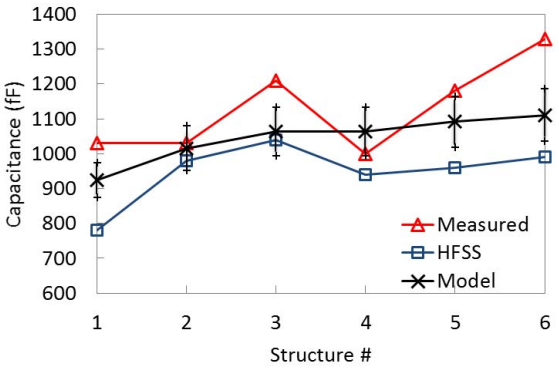

Fig. 7. Low-frequency capacitance of different TSV array configurations.

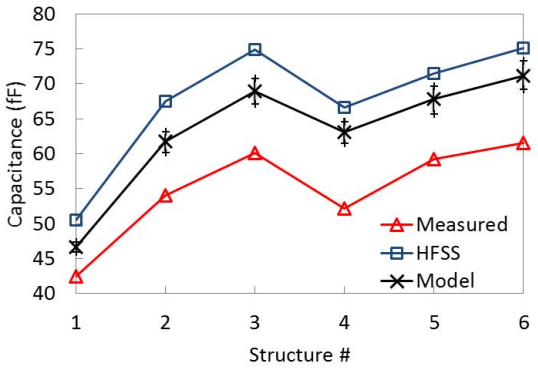

Fig. 8. High-frequency capacitance of multiple TSV array configurations, for a TSV pitch of 100 μm.

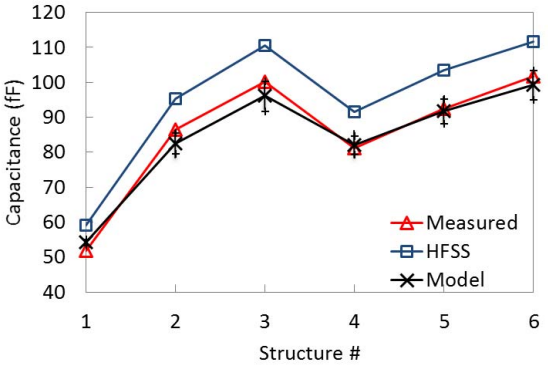

Fig. 9. High-frequency capacitance of multiple TSV array configurations, for a TSV pitch of 50 μm.

The effective capacitance obtained through this model is compared with experimental results. The error in the low-frequency model is <17%, as shown in Fig. 7. At a TSV pitch of 100-μm and at high frequency, although the maximum error is approximately 21% for structure 4, the trend of capacitance values is well matched between the model, simulation, and measurements, as shown in Fig. 8. For a TSV pitch of 50 μm, the model has an error of <5%, as shown in Fig. 9. It is worth noting that for all six structures, the 50-μm pitch TSVs have larger high-frequency capacitance than the 100-μm pitch TSVs due to the larger impact of substrate capacitance at high frequencies, which is consistent with the result in [13].

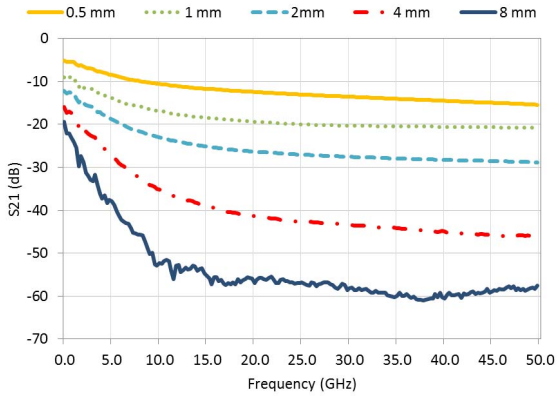

Fig. 10. Measured S_{21} of TSV-wire-TSV links for five different wire lengths.

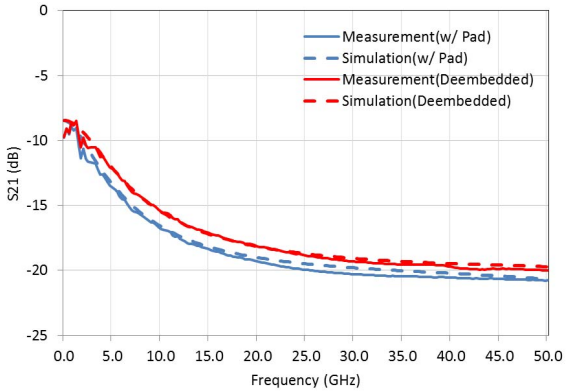

Fig. 11. Measured and simulated S21 before and after de-embedding for TSV-wire-TSV links with a wire length of 1 mm.

B. 3-D IC Links

Five sets of links with different wire lengths are measured, and the results are shown in Fig. 10. The loss increases with frequency and wire length as expected. It is evident that the loss of these links is large even at low frequency. The insertion loss of the 1-mm long link at 10 MHz is as high as −9.75 dB. This is due to the high dc resistance of the wires. It should also be noted that the measurement of the 8-mm-long wire exhibits some noise, which is believed to be due to the small values of S_{21}.

The L-2L de-embedding method is adopted to eliminate the probe pads [22]. Fig. 11 shows the originally measured S_{21}, the de-embedded S_{21}, and the values obtained via HFSS simulations of a 3-D IC link. The HFSS simulations correlate well with the measurements, with an average difference of 1.25%.

After de-embedding the probe pads, the effective link consists of two TSVs interconnected with a wire, i.e., a TSV-wire-TSV link. Next, the TSVs are de-embedded to obtain the S-parameters of only the wire (TSVs on both sides are de-embedded), the wire-TSV link (the TSV on the driver

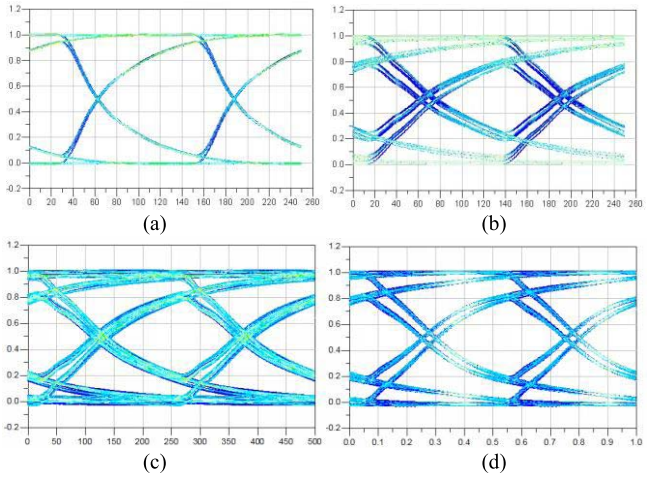

Fig. 12. Eye diagrams of four structures with different wire lengths. (a) 0.5 mm at data rate of 8 Gb/s. (b) 1 mm at 8 Gb/s. (c) 2 mm at 4 Gb/s. (d) 4 mm at 2 Gb/s.

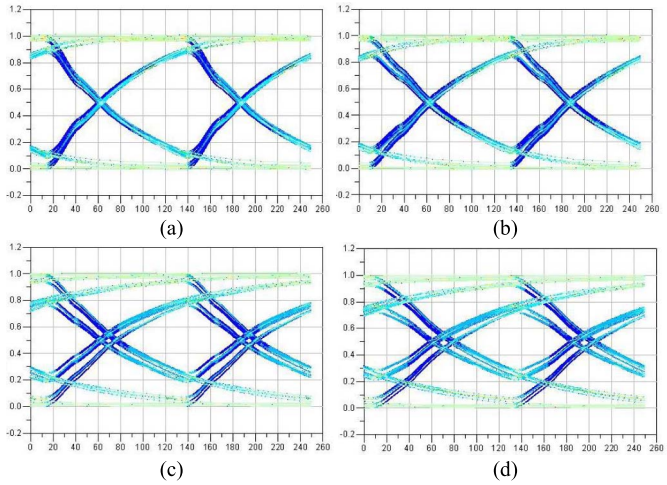

Fig. 13. Eye diagrams of the four structures (a) wire only, (b) TSV-wire, (c) Wire-TSV, and (d) TSV-wire-TSV for 1-mm wire length at data rate of 8 Gb/s.

side is de-embedded), and the TSV-wire link (the TSV on the receiver side is de-embedded).

The S-parameters are imported into Keysight ADS to extract the eye diagram and delay. The driver resistance and receiver capacitance are from the ITRS 2013 14-nm node [21]. The eye diagrams for wire-TSV links are shown in Fig. 12. At a data rate of 8 Gb/s, the eye is closed for links longer than 2 mm. However, they can still achieve an eye-opening of 50% at lower bit rates, as shown Fig. 12(c) and (d). Fig. 13 shows the impact of the TSV by comparing four structures of the same wire length at a date rate of 8 Gb/s. Compared with the wire-TSV link shown in Fig. 13(c), the TSV-wire link in Fig. 13(b) improves the eye opening from 510 to 650 mV. This demonstrates that the performance of the link is improved when the TSV is placed closer to the driver. The reduced eye opening of the wire-TSV link is due to the interaction of the driver side wire resistance and the TSV capacitance. By placing the TSV closer to the driver, the driver side wire resistance becomes smaller, and therefore, a larger eye opening is achieved.

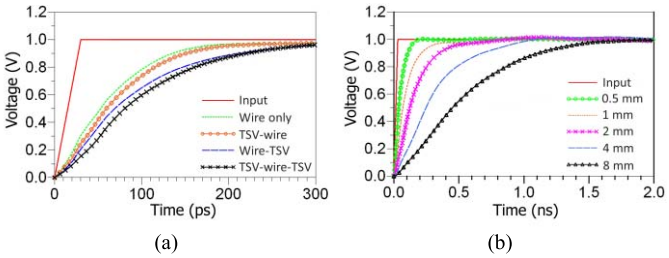

Fig. 14. Step response of (a) TSV-wire-TSV, wire-TSV, TSV-wire, and wire only for 1-mm wire length and (b) five links with different wire length: 0.5, 1, 2, 4, and 8 mm.

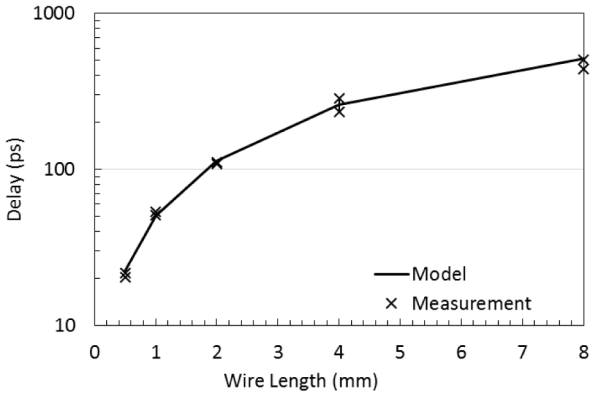

Fig. 15. Modeled and measured delay as a function of wire length.

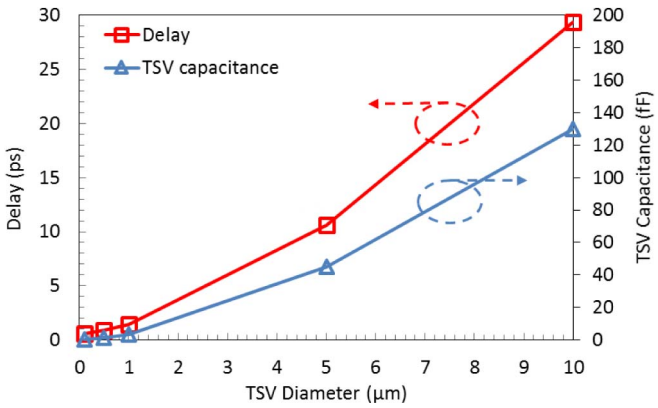

Fig. 16. Impact of TSV geometry scaling on TSV capacitance and link delay.

Fig. 14(a) shows the step response of four links with the same wire length. Compared with the wire only 50%–50% delay of 37.6 ps, the delay of the wire-TSV link is 53.9 ps, an increase of 43.4% due to the presence of the TSV. Moving the TSV to the driver side (e.g., TSV-wire link) decreases the delay to 44.5 ps, an improvement of 17.4% and an increase of 18.4% compared with the wire only case. Fig. 14(b) shows the response of the wire-TSV link for five different wire lengths.

The delay of the wire-TSV link at five different wire lengths is modeled using the analytical model presented in Section II and compared with measurements, as shown in Fig. 15. For each wire length, we measured two identical structures and the results are marked as crosses. In the model, the wire resistance, wire capacitance, and TSV capacitance values are extracted

from the measurements. The maximum difference between the modeled and measured delays is approximately 8.5% at a wire length of 8 mm. Even though the wires are longer than typical on-chip wires, the time of flight was ignored in the model due to the high resistance of the wires [24].

The impact of TSV geometry scaling on the TSV capacitance and link delay is analyzed with the verified models, as shown in Fig. 16. In this analysis, the TSV aspect ratio is assumed to be 10:1. Moreover, the silicon dioxide liner thickness is assumed to be 1/10 of the TSV diameter, and the M1 wire length is set to 10 μm. The link delay decreases significantly as the TSV diameter decreases. When the TSV diameter scales below 1 μm, the link delay becomes saturated. This is because the TSV capacitance becomes comparable with the on-chip wire capacitance, and the delay begins to be dominated by the on-chip wires.

V. Conclusion

In this paper, TSV arrays and 3-D IC links with TSVs and horizontal wires are fabricated, measured, and analyzed. The TSV capacitance and link delay models are verified with measurements. It is shown that the TSV capacitance and the driver side wire resistance can dominate the link performance and could potentially be the key bottleneck for digital 3-D ICs. The delay and eye opening of the link can be significantly improved by placing TSVs closer to their drivers. As presented in Part I and Part II, reducing the length of on-chip wires and height and diameter of the TSVs have a significant impact on 3-D IC link performance.

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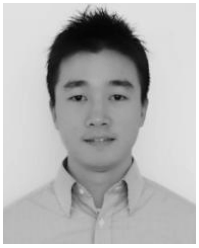

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